II. REMARKS

Claims 1-38 are pending. The Applicants' attorney has cancelled claims 15 and 22 and has amended claims 11 and 20. But this amendment adds no new matter to the patent application. In light of the following, all of the claims as amended are now in condition for allowance, and, therefore, the Applicants' attorney requests the Examiner to withdraw all of the outstanding rejections. But if after considering this response the Examiner does not allow all the claims, the Applicant's attorney requests that the Examiner contact him to schedule a teleconference to further the prosecution of the application.

Rejection of Claim 38 Under 35 U.S.C. § 102(e) As Being Anticipated by U.S. 2002/0110037 to Fukuyama et al.

Claim 38 recites an address counter operable to generate an internal address and a comparator operable to compare an external address to the internal address.

For example, referring to FIGS. 3-5 and pages 6-11 of the patent application, a memory 26 includes a column address bus (*e.g,* the output of the column address buffer 44) that receives an external column address from a processor 64 (FIG. 6) or other source external to the memory 26, a column-address anticipation counter 14 operable to generate an internal column address, and a comparator 18 operable to compare the external column address to the internal column address.

In contrast, Fukuyama does not disclose comparing an external address to an internal address generated by an address counter. Referring, *e.g.*, to FIG. 7 and paragraph [0119] of Fukuyama, although the comparator 45 compares an internal address from an address counter 42 to a preprogrammed final column address (*e.g.,* 111111), the final column address is not an external adress.

Rejection of Claims 1-17 and 20-37 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Fukuyama in view of U.S. Patent 6,128,716 to Biggs

Claim 1

Claim 1 recites a comparator operable to compare an external address to a value, and a control circuit operable to terminate a data-transfer cycle based on the relationship between the external address and the value.

For example, referring to FIGS. 3-5 and pages 6-11 of the patent application, a memory 26 includes a column address bus (*e.g,* the output of the column address buffer 44) that receives an external column address from a processor 64 (FIG. 6) or other source external to the memory 26, and a comparator 18 operable to compare the external column address to a value. A control circuit 24 terminates a read or a write cycle based on the relationship between the external address and the value. Examples of this value include the interal column address from the counter 14 and the contents of the page-length register/counter 16. For example, per the timing diagram of FIG. 3, the control circuit 24 terminates a read cycle when the external address does not equal the internal address, and enables the read cycle when the external address equals the internal address.

In contrast, the combination of Fukuyama and Biggs does not suggest comparing an external address to a value and terminating a data-transfer cycle based on the relationship between the external address and the value.

The Examiner agrees that Fukuyama does not disclose terminating a data-transfer cycle based on a relationship between an external address and a value.

Furthermore, Biggs lacks the teaching missing from Fukuyama, namely terminating a data-transfer cycle based on a relationship between an external address and a value. Referring, *e.g.*, to FIGS 1-3 and col. 3, line 48 – col. 4, line 12, Biggs claims to eliminate the precharge penalty previously associated with page-mode memory accesses. Referring to FIG. 3, during a current bus cycle 2, a memory controller 42 recieves from a processor 41 an address R2C2 of a DRAM 43,

where R2 is the page (*i.e.*, row) address and C2 is the column address. Also during this current bus cycle, the memory controller 42 stores R2 in a register 60 and receives from the processor 41 an address R3C3, which is the address for the next bus cycl 3. A page hit comparator 62 compares R3 to the stored R2. If R3C3 is on the same "page" as R2C2, that is, if R3 = R2 (page hit), then no precharge of another row is required; conversely, if R3C3 is on a different "page" from R2C2, that is, if R3 $\neq$R2 (no page hit), then the row corresponding to the page of R3 must be precharged by transitioning RAS* to an inactive high level during bus cycle 2 as shown in FIG. 3. By so transitioning RAS* during bus cycle 2, the new row is fully precharged by the start of bus cycle 3, thus preventing delay in the commencemnt of bus cycle 3. Consequently, the controller 42 determines whether to precharge a row of the DRAM memory 43 based on the comparison of the external address (*e.g.,* R3) to a value (*e.g.,* R2). But the controller 42 does not terminate a data-transfer cycle based on this comparison. Only the processor 41 can initiate and terminate data-transfer cycles via the control signals it generates (CONTROL bus of FIG. 1). Because the processor 41 does not receive the output (page hit) from the comparator 62, the processor does not and cannot terminate a data-transfer cycle based on the relationship between the external address and the page stored in the register 60. Therefore, although Biggs discloses precharging a row based on a relationship between an external address and a value (page stored in the register 60), he neither discloses nor suggests terminating a data-transfer cycle based on such a relationship.

Moreover, not only would one not have been motivated to combine the teachings of Fukuyama and Biggs to arrive at the subject matter recited in claim 1, but he would have been motivated away from such combination. Bigg's technique can be used only in systems having a processor that can provide a next address before the current data-transfer cycle is finished executing. Fukuyama's technique anticipates the next address, and thus can be used where preaddressing is not available. Consequently, because Bigg's techique cannot be used in the type of system for which Fukuyama developed his technique, one would realize that combining Bigg's technique with Fukuyama's techique would yield no useful result.

Claims 2-10

These claims are patentable by virtue of their dependencies from claim 1.

Claim 11

Claim 11 as amended recites an address counter operable to generate an internal address during a data-transfer cycle, a comparator operable to compare the internal address to an address value, and a control circuit operable to terminate the data-transfer cycle when the internal address has a predetermined relationship to the address value.

For example, referring to FIGS. 3-5 and pages 6-11 of the patent application, a memory 26 includes a column-address anticipation counter 14 for generating an internal column address, a page-length register/counter 16 (storage circuit) for receiving and storing an address value, a comparator 18 operable to compare the internal column address to the address value, and a control circuit 24 for terminating a read or a write cycle when the internal address has a predetermined relationship to the address value. For example, the register/counter 16 may store an ending address, and, per the timing diagram of FIG. 3, the control circuit 24 terminates a read cycle when the internal address equals the stored ending address, and enables the read cycle when the internal address does not equal the stored ending address.

In contrast, the combination of Fukuyama and Biggs does not suggest a comparator operable to compare an internal address generated by an address counter to an address value, and a control circuit operable to terminate the data-transfer cycle when the internal address has a predetermined relationship to the address value.

The Examiner agrees that Fukuyama does not disclose terminating a data-transfer cycle when an internal address generated by Fukuyama's address counter 42 has a predetermined relationship to the final column address value stored in Fukuyama's comparator 45.

Furthermore, Biggs lacks the teaching missing from Fukuyama, namely terminating a data-transfer cycle when an internal address generated by an address

counter has a predetermined relationship to an address value. Referring, *e.g.*, to FIGS 1-3, Biggs neither discloses nor suggests an address counter.

Moreover, not only would one not have been motivated to combine the teachings of Fukuyama and Biggs to arrive at the subject matter recited in claim 11, but he would have been motivated away from such combination for the reasons rectied above in support of the patentablity of claim 1.

Claims 12-17

These claims are patentable by virtue of their dependencies from claim 11.

Claim 20

Claim 20 as amended is patentable for reasons similar to those recited above in support of the patentability of claim 11.

Claims 21-22

These claims are patentable by virtue of their dependencies from claim 20.

Claim 23

Claim 23 recites comparing a received address to a generated address and terminating a cycle during which data is being transferred to or from a storage location residing at the generated address if the received address does not have a predetermined relationship to the generated address.

For example, referring to FIGS. 3-5 and pages 6-11 of the patent application, a comparator 18 compares a received external column address with an internal column address generated by a counter 14, and a column decoder 38 transfers data to/from a location of the array 30 residing at the internal column address. A control circuit 24 terminates this data-transfer cycle if the external column address does not have a predtermined relationship to the internal column address. For example, per

the timing diagram of FIG. 3, the control circuit 24 may terminate the data-transfer cycle if the internal column address does not equal the external column address.

In contrast, the combination of Fukuyama and Biggs does not suggest comparing a received address to a generated address and terminating a data-transfer cycle if the received address does not have a predetermined relationship to the generated address.

Fukuyama does not disclose or suggest comparing a received address to a generated address and terminating a data-transfer cycle if the received address does not have a predetermined relationship to the generated address. Referring, *e.g.*, to FIG. 7 and paragraph [0050] of Fukuyama, none of the comparators 24, 25, and 45 compare the received external address from the address decoder 21 to the internal address generated by the address counter 42. In addition, the Examiner agrees that Fukuyama does not disclose terminating a data-transfer cycle if the received address does not have a predetermined relationship to the generated address.

Furthermore, for reasons similar to those recited above in support of the patentability of claim 1, Biggs lacks a teaching missing from Fukuyama, namely terminating a data-transfer cycle if a received address does not have a predetermined relationship to a generated address.

Moreover, not only would one not have been motivated to combine the teachings of Fukuyama and Biggs to arrive at the subject matter recited in claim 23, but he would have been motivated away from such combination for the reasons recited above in support of the patentablity of claim 1.

Claims 24-26

These claims are patentable by virtue of their dependencies from claim 23.

Claim 27

Claim 27 is patentable for reasons similar to those recited above in support of the patentability of claim 11.

Claims 28-33

These claims are patentable by virtue of their dependencies from claim 27.

Claim 34

Claim 34 recites loading a memory with a count value from an external source, generating a first address inside of the memory, the first address being distinct from the count value, incrementing or decrementing the count value, comparing the count value to a predetermined value, and terminating a cycle during which data is being transferred to or from a storage location residing at the first address if the count value has a predetermined relationship to the predetermined value.

For example, referring to FIGS. 3-6 and pages 6-11 of the patent application, a register/counter 16 is loaded with a count value from an external source such as a processor 64, a column-address anticipation counter 14 generates an internal column (first) address that is distinct from the count value in the register/counter 16, the register/counter 16 increments or decrements the count value, the comparator 18 or the control circuit 24 compares the count value to a predetermined value, and the control circuit 24 terminates the data-transfer cycle during which data is transferred to or from the location(s) in the array 30 at the internal column address(es) if the count value equals the predetermined value.

In contrast, the combination of Fukuyama and Biggs does not suggest loading a count value from an external source, generating an address that is distinct from the count value, incrementing or decrementing the count value, ornot terminating a cycle during which data is being transferred to or from a storage location residing at the address if the count value has a predetermined relationship to a predetermined value.

Fukuyama does not load a count value from an external source and generate an address that is distinct from the count value, does not increment or decrement the

count value, and does not terminate a cycle during which data is being transferred to or from a storage location residing at the address if the count value has a predetermined relationship to a predetermined value. Referring, *e.g.*, to FIG. 7, Fukuyama's address counter 42 generates an address, but nowhere does Fukuyama load from an external source a count value that is distinct from the address generated by the counter 42. Consequently, Fukuyama's circuitry cannot increment/decrement such a count value, or terminate a data-transfer cycle in response to such a count value. The Examiner agrees Fukuyama does not disclose or suggest terminating a data-transfer cycle in response to an externally loaded count value.

Furthermore, Biggs lacks the teachings missing from Fukuyama, namely loading a count value from an external source and generating an address that is distinct from the count value, incrementing or decrementing the count value, and terminating a cycle during which data is being transferred to or from a storage location residing at the address if the count value has a predetermined relationship to a predetermined value. Nowhere does Biggs disclose or suggest a count value. In addition, for reasons similar to those recited above in support of the patentability of claim 1, Biggs neither discloses nor suggest terminating a data-transfer cycle based on a relationship between two values such as a count value and a predetermined value.

Moreover, not only would one not have been motivated to combine the teachings of Fukuyama and Biggs to arrive at the subject matter recited in claim 34, but he would have been motivated away from such combination for the reasons recited above in support of the patentablity of claim 1.

Claims 35-37

These claims are patentable by virtue of their dependencies from claim 34.

Rejection of Claims 18-19 Under 35 U.S.C. § 103(a) as Being Unpatentable Over Fukuyama In View Of U.S. Patent 6,484,231 to Kim

Claim 18

Claim 18 recites an address bus operable to receive an external address, an address counter operable to generate an internal address, an address decoder, and a multiplexer coupled to the address bus, the address counter, and the address decoder and operable to couple either the external address or the internal address to the address decoder.

For example, referring to FIGS. 4-5 of the patent application, a memory circuit 26 includes an address bus (input of column address buffer 44) for receiving an external column address, an address counter 14 for generating an internal column address, a column-address decoder 38, and a multiplexer 22 for coupling either the external column address or the internal column address to the column-address decoder 38.

In contrast, the combination of Fukuyama and Kim does not suggest a multiplexer operable to couple either an external address or internal address to an address decoder. Referring, *e.g.,* to Fukuyama's FIG. 7, Fukuyama does not disclose a multiplexer. Referring to Kim's FIG. 4, although Kim discloses a multiplexer 100, this multiplexer does not couple any address to the address decoder 50, but instead couples data to/from a selected cell block 61-64 from/to data I/O pads 9 via respective sense amplifiers 71-74 to speed up the writing and reading of data. Therefore, the combination of Fukuyama and Kim would at most suggest incorporating Kim's data I/O multiplexer 100 between Fukuyama's I/O pads and sense amplifiers (neither shown in Fukuyama), and would not suggest adding to Fukuyama's circuit a multiplexer that couples either the external address (input to the address decoder 21) or the internal address from the address counter 42 to the address decoder 21.

The Applicants' attorney does not understand the Examiner's position in section 10 of the Office Action, because Kim's multplexer 100 couples only data from

one component (register 8) to another component (I/O pad 9), and clearly does not couple addresses to the address decoder 50 or to any other components.

Conclusion

In light of the foregoing, claims 1-10, 12-14, 16-19, 21, and 23-38 as previously pending, and claims 11 and 20 as amended, are in condition for full allowance, which is respectfully requested.

In the event additional fees are due as a result of this amendment, payment for those fees has been enclosed in the form of a check. Should further payment be required to cover such fees you are hereby authorized to charge such payment to Deposit Account No. 08-2025.

DATED this 20th day of December, 2004.

Respectfully Submitted,

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